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Abstract
In recent years, studies about Double-Gate (DG) transistor have successively been proposed, and have attracted a lot of attention. As CMOS is scaled to the limit, dou-ble-gate (DG) MOSFET becomes increasingly important. A number of authors have ap-plied various simplifying assumptions to model the SCE of DG fully-depleted MOS-FETs analytically. Some of them make use of a parabolic potential approximation ap-proach for the device in the direction perpendicular to the surface. This results in a scale length proportional to the oxide and the silicon thickness. Large errors occur when one of thickness is much less than the other. Other approaches apply the superposition method to solve the 2-D boundary-value problem for the bulk MOSFETs. Most of them only put focus on device scaling scheme, threshold degradation by ignoring the 2-D ef-fects in the gate oxide. In order to give insight into the device physics, we need to de-velop a consolidated threshold voltage model for the DG transistor with fully 2-D ef-fects included in both silicon and gate oxide regions.
In this thesis, we successfully develop a physical and analytical threshold voltage model for fully depleted Asymmetric DG MOSFETs by use of the 2-D analytical solu-tion in the entire region of the device based on fully closed-form solutions of Poisson's equation in both regions of Si body and gate insulator. Without any fitting parameters, these analytical results are useful in predictive compact modeling of Asymmetric DG MOSFETs. The model shows the distribution of electric potential, short channel thresh-old voltage roll-off (ΔVTH), subthreshold current, subthreshold slope (Swing) and drain-induced barrier lowering (DIBL) effects. The new model is verified by published numerical simulations with close agreement. Due to its computational efficiency, this model can be applied for SPICE simulation.
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